AMENDMENTS TO THE CLAIMS

This listing of claims replaces all prior listing of claims in this application.

Claims 1-21 (Canceled).

22. (Currently amended) A transistor structure comprising:

a semiconductor substrate;

a gate stack with sidewalls provided over said substrate, said gate stack comprising:

a gate oxide layer provided over said substrate;

a polysilicon layer provided over said gate oxide layer;

at least one insulating ~~spacers~~ spacer provided over said polysilicon layer;

at least one channel implant region formed underneath said gate stack, wherein said at least one insulating ~~spacers define~~ spacer defines at least in part the at least one channel implant region; and,

source and drain regions provided in said substrate on opposite sides of said gate stack.

23. (Currently amended) A structure as in claim 22, wherein [[said]] at least another insulating ~~spacers are~~ spacer is formed on ~~the sidewalls~~ a sidewall of said gate stack.

24. (Canceled).

25. (Currently amended) A structure as in claim 23, wherein said at least one channel implant region is defined at least in part by said at least another sidewall ~~spacers~~ spacer and is approximately the same width as said gate stack.

26. (Currently amended) A structure as in claim [[24]] 22, wherein said at least one channel implant region is defined at least in part by said at least one insulating ~~spacers~~ spacer and is narrower than the width of said gate stack.

27. (Currently amended) A structure as in claim 23, further comprising an insulating layer adjacent to said at least another sidewall ~~spacers~~ spacer, said insulating layer and said at least another sidewall ~~spacers~~ spacer having at least a portion of their upper surfaces removed to define an area extending beyond a lateral width of said gate stack.

28. (Previously presented) A structure as in claim 27, wherein said at least one channel implant region is defined at least in part by said area.

29. (Canceled).

30. (Currently amended) A structure as in claim [[29]] 25, further comprising a second channel implant region formed in said at least one channel implant region, which is defined at least in part by said ~~second~~ at least one insulating ~~spacers~~ spacer provided over said polysilicon layer.

Claims 31-32 (Canceled).

33. (Previously presented) A structure as in claim 22, further comprising a silicide layer formed over said gate stack, wherein said silicide layer is formed of a material selected from the group consisting of W, WSi_x, WN, Ti, TiN, and other combinations thereof.

Claims 34-69 (Canceled).

70. (Previously presented) A transistor structure comprising:

a semiconductor substrate;

a gate stack with sidewalls provided over said substrate, said gate stack comprising:

a gate oxide layer provided over said substrate;

a conducting layer provided over said gate oxide layer;

sidewall spacers provided adjacent to the sidewalls of said gate stack;

an insulating layer formed adjacent to said sidewall spacers, said insulating layer and sidewall spacers having etched out upper portions that define an area extending beyond a lateral width of said gate stack; and

at least one channel implant region formed beneath said gate stack, which is defined at least in part by said area, wherein said at least one channel implant region is wider in width than said gate stack.

71. (Original) A structure as in claim 70, wherein said conducting layer is polysilicon.

Claims 72-73 (Canceled).

74. (Previously presented) A structure as in claim 70, further comprising a silicide layer formed over said gate stack, wherein said silicide layer is formed of a

material selected from the group consisting of W, WSi_x, WN, Ti, TiN, and other combinations thereof.

75. (Previously presented) A transistor structure comprising:

a semiconductor substrate;

a gate stack with sidewalls provided over said substrate, said gate stack comprising:

a gate oxide layer provided over said substrate;

a conducting layer provided over said gate oxide layer;

first sidewall spacers provided adjacent to the sidewalls of said gate stack;

second sidewall spacers provided over said conducting layer; and

at least one channel implant region formed underneath said gate stack, which is defined at least in part by said second sidewall spacers, wherein said at least one channel implant region is narrower in width than said gate stack.

76. (Original) A structure as in claim 75, wherein said conducting layer is polysilicon.

77. (Previously presented) A structure as in claim 75, further comprising an insulating layer formed adjacent to said first sidewall spacers, said insulating layer and said first sidewall spacers having removed portions that define an area extending beyond a lateral width of said gate stack.

78. (Previously presented) A structure as in claim 77, wherein a second channel implant region is formed beneath said gate stack, which is defined at least in part by said area, wherein said second channel implant region is wider in width than said gate stack.

79. (Previously presented) A structure as in claim 77, further comprising a silicide layer formed over said gate stack, wherein said silicide layer is formed of a material selected from the group consisting of W, WSi_x, WN, Ti, TiN, and other combinations thereof.

80. (Previously presented) A transistor structure comprising:

a semiconductor substrate;

a gate stack with sidewalls provided over said substrate, said gate stack comprising:

a gate oxide layer provided over said substrate;

a conducting layer provided over said gate oxide layer;

first sidewall spacers provided adjacent to the sidewalls of said gate stack;

an insulating layer formed adjacent to said first sidewall spacers that defines an area extending beyond a lateral width of said gate stack;

a first channel implant region formed underneath said gate stack, which is defined at least in part by said area; and

a second channel implant region formed within said first channel implant region.

81. (Original) A structure as in claim 80, wherein said conducting layer is polysilicon.

Claims 82-83 (Canceled).

84. (Previously presented) A structure as in claim 80, further comprising a silicide layer formed over said gate stack, wherein said silicide layer is formed of a material selected from the group consisting of W, WSi_x, WN, Ti, TiN, and other combinations thereof.

85. (Previously presented) A transistor structure comprising:

a semiconductor substrate;

a gate stack with sidewalls provided over said substrate, said gate stack comprising:

a gate oxide layer provided over said substrate;

a conducting layer provided over said gate oxide layer;

first sidewall spacers provided adjacent to the sidewalls of said gate stack;

a first channel implant region formed underneath said gate stack, which is defined at least in part by said first sidewall spacers;

second sidewall spacers provided over said conducting layer;

a second channel implant region formed within said first channel implant region, which is defined at least in part by said second sidewall spacers.

86. (Previously presented) A structure as in claim 85, further comprising a silicide layer formed over said gate stack, wherein said silicide layer is formed of a material selected from the group consisting of W, WSi_x, WN, Ti, TiN, and combinations thereof.

Claims 87-91 (Canceled).

92. (Previously presented) A gate stack with sidewalls for use in a MOSFET, said gate stack comprising:

an oxide layer provided over a semiconductor substrate;

a conducting layer provided over said oxide layer;

a first set of spacers provided on each side of said gate stack with a second set of spacers provided over said conducting layer; and

a first channel implant region formed underneath said gate stack and in said semiconductor substrate, wherein the first set of spacers or second set of spacers define at least in part the width of said channel implant region.

93. (Previously presented) The gate stack structure of claim 92, wherein said first set of spacers are formed on the sidewalls of said gate stack.

94. (Previously presented) The gate stack structure of claim 93, wherein said first channel implant region is formed self-aligned to said gate stack.

95. (Previously presented) The gate stack structure of claim 94, further comprising a second channel implant region formed within the first channel implant

region, wherein said second channel implant region is narrower in width than said first channel implant region.

96. (Previously presented) The gate stack structure of claim 92, wherein said second set of spacers are formed over said conducting layer.

97. (Previously presented) The gate stack structure of claim 96, wherein said first channel implant region is narrower in width than said gate stack.

98. (Previously presented) The gate stack structure of claim 92, further comprising an insulating layer formed adjacent to said first set of spacers, wherein said insulating layer and said first set of spacers have etched out portions that define an area extending beyond a lateral width of said gate stack.

99. (Previously presented) The gate stack structure of claim 98, wherein said first channel implant region is wider than said gate stack.

100. (Previously presented) The gate stack structure of claim 98, further comprising a second channel implant region formed within said first channel implant region.